Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1 OUT**
2. **1 IN -**
3. **1 IN +**
4. **VCC -**
5. **2 IN +**
6. **2 IN -**
7. **2 OUT**
8. **VCC +**

**MASK**

**REF**

**2**

**3**

**1 8 7**

**6**

**5**

**4**

**.078”**

**.096”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .078” X .096” DATE: 7/27/16**

**MFG: LINEAR TECH THICKNESS .014” P/N: LT1013**

**DG 10.1.2**

#### Rev B, 7/1